Comparison of Space Vector and Carrier Based Pulse Width Modulation Technique for Three Level Inverter

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Abstract— This paper presents two different PWM techniques: the sinusoidal PWM (SPWM) technique, and the space-vector PWM (SVPWM) technique for three level voltage source inverter. These two methods are compared by discussing their ease of implementation and by analyzing the output harmonic spectra of various output voltages (poles voltages, line-to-neutral voltages, and line-to-line voltages) and their total harmonic distortion (THD).Simulation results for both the method is presented here.

Index Terms— Voltage source inverter, Space Vector PWM, 3-Level Invertert; sine pulse width modulation (SPWM), Total harmonic distortion.(THD), voltage level redundancy

1 Introduction

In recent years, multilevel inverters are gaining more and more attention in the application areas of medium voltage and high power due to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current. Comparing two-level inverter topologies at the same power ratings, MLIs also have the advantages that the harmonic components of line-to-line voltages. [1] Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM) used Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM) there are many techniques [3] [4], which are applied to multilevel inverter topologies. PWM inverters can control their output voltage and frequency simultaneously. And also they can reduce the harmonic components in load currents [5]. These features have made them favourable in many industrial applications such as variable speed drives, uninterruptible power supplies, and other power

This paper discusses the advantages and drawbacks of two different PWM techniques: the sinusoidal PWM (SPWM) technique and the space-vector PWM (SVPWM) technique used for three level voltage source inverter. In section II various common multilevel inverter topologies discussed in brief. Section III discussed SPWM and SVM techniques used for three level inverter. Section IV simulation results for both PWM methods followed by discussion.

2 Inverter Topologie

Figure 1 shows three different topologies proposed for multilevel inverters: diode-clamped (neutral-clamped) [3]; capacitor-clamped (flying capacitors) and cascaded multicell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).

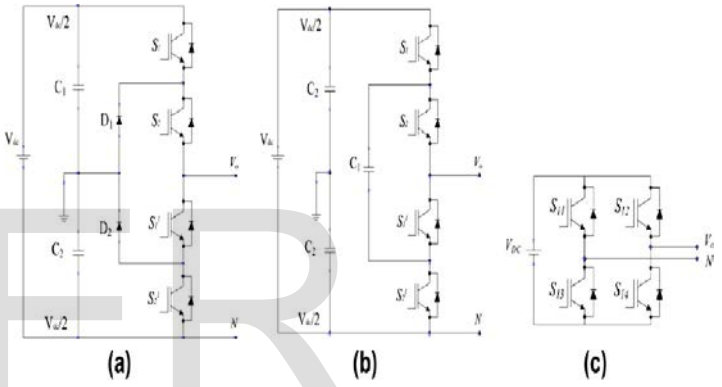

Fig.1. Multilevel inverter topologies: (a) three-level DC-MLI, (b) three-level FC-MLI, (c) three-level CHB-MLI

2.1 Three level neutral point clamped inverter

Three-level inverter has the advantages of having low harmonic distortion, low switching frequency, and lower common mode voltages, near sinusoidal output voltage less requirement of filtering and above all it reduces the danger of motor failure due to high frequency switching dv/dt and . Fig (1) shows three-phase three level diode clamped inverter. It consists of capacitors, switching devices, dc voltage source and clamping diodes. Middle point of two capacitors is confined as neutral point. The output voltage has three states.

Vdc/2, 0 and - Vd&/2 for 3-level NPC or five states: Vdc, 3Vdc/4, Vdc/2, Vd&/4 and 0. To synthesize 3-level output phase voltage, switching sequence as given in Table I will be used. Table gives the switch states for a-phase. Similar switching sequence will be derived for other phases taking into account for phase delays among phases. Thus three level inverter is used in high voltage, high power ac drives. State condition 1 means switch ON and 0 means switch OFF. Fig 2 shows the phase and line voltage of 3-level diode clamped VSI. Now, it is clear that an m -level diode clamped VSI. Now, it is clear that an m -level diode clamped inverter consists of (m-1) capacitors on dc bus, output phase voltage has m-levels and output line voltage has (2m-1)-levels. Each active switching device has to withstand a blocking voltage of Vdc/(m-1), even then clamping diode must have different voltage ratings for reverse

voltage blocking. The number of diodes required for each phase will be (m-1) x (m-2).

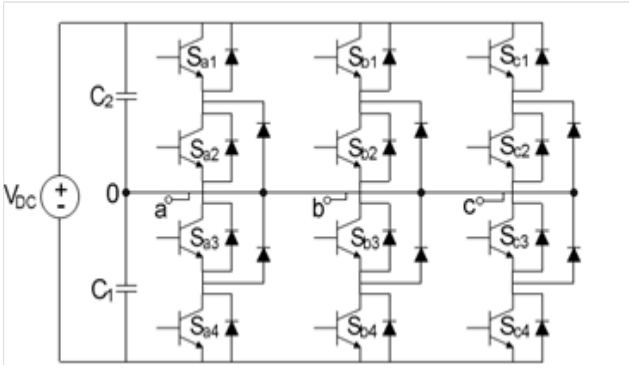

Fig 2 Three-phase, Three-Level Diode Clamped Inverter

From Table I, it is clear that when both the upper switches Sa_1 and Sa_2 are closed, full supply voltage will be available across the load. If two central switches Sa_2 and Sa_3 are closed then half of dc supply voltage will be obtained and zero voltage will be applied across load if lower switches Sa_3 and Sa_4 are closed.

Table-I
SWITCHING STATE FOR THREE LEVEL NPC

Switch status	State	Output voltage
Sa_1=on,Sa_2=on Sa_3=off,S_{a4}=off	Mode1	Vao=+Vdc/2
Sa_2=on,Sa_3=on Sa_1=off,S_{a4}=off	Mode2	Vao=0
Sa_3=on,S4=on Sa_1=off,Sa_2=off	Mode 3	Vao=-Vdc/2

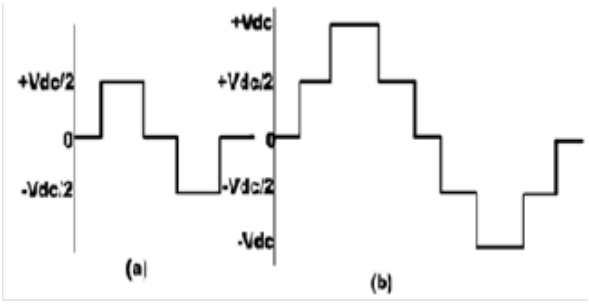

Fig 3 Output voltages in three-level diode- clamped inverter (a) Phase voltage (b) Line voltage

2.2 Flying Capacitor Converters

The FC topology is in some way similar to the NPC ,with the main difference being that the clamping diodes are replaced by flying capacitors, as can be seen in Fig. 4. Here the load cannot be directly connected to the neutral of the converter to generate the zero voltage level. Instead, the zero level is obtained by connecting the load to the positive or negative bar through the flying capacitor with opposite polarity respect the dc-link. Like with the NPConly two gating signals are necessary per phase to avoid dc link and flying capacitor short-circuit. However, in the FC, the inverted gating signals are related to different switching devices. Another difference with the NPC is that the four combinations of (Sa_1, Sa_2)are allowed. Only three are shown in Fig. 4. The middle circuit in Fig. 4 shows (Sa_1, Sa)=(1,0) which generates the zero level. The same level is obtained with (Sa1, Sa) =(0,1) This property is known as voltage level redundancy and can be used for control or optimization purpose

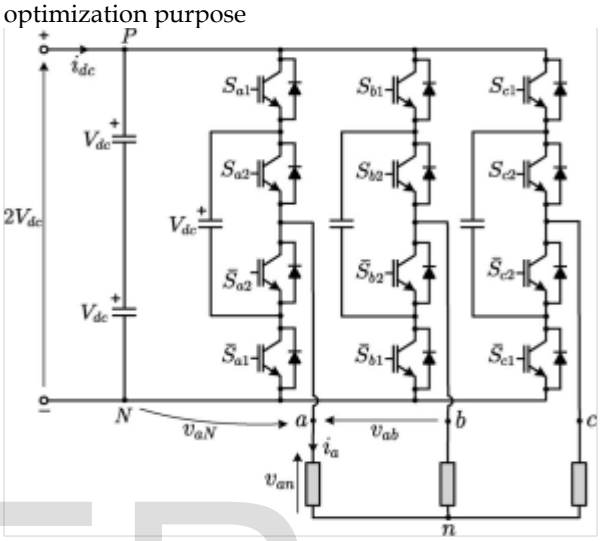

Fig 4 Three-phase, Three-Level Flying capacitor Inverter

2.3 Cascaded H-Bridge Converters

A three phase cascaded multilevel inverter is shown in Fig.5 The circuit is designed for a five-level inverter consisting of 12 switches. Each DC source connected with its respective H-bridge, and generates three different output voltages, +Vdc, 0, and –Vdc, using various combinations of switching. The output of the multilevel inverter is synthesized by H-bridges connected in series. The number of output phase voltage levels in a cascaded inverter is given as m=2s+1, where s is the number of separate DC sources and m is the inverter.

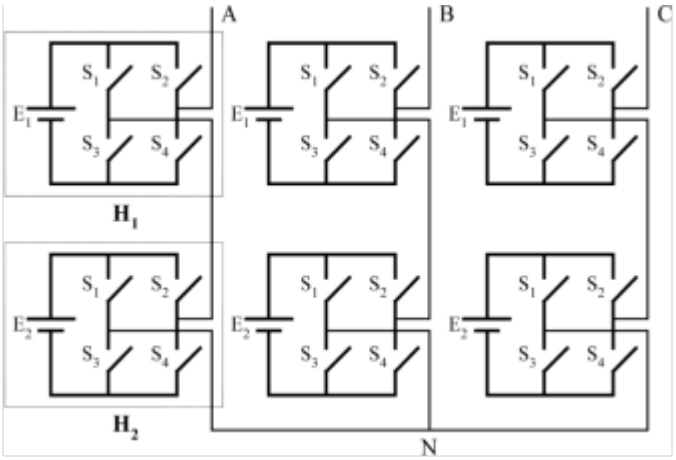

Fig 5 Three-phase fivee-Level Cascaded Inverte

3 SPWM AND SVM TECHNIQUES

Multilevel inverter control techniques are based on fundamental and high switching frequency. Three main control techniques of multilevel inverters are SHE-PWM,SPWM and SVPWM.

3.1. Sinusoidal Pulse Width Modulation (SPWM)

SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Power dissipation is one of the most important issues in high power applications. The fundamental frequency SPWM control method was proposed to minimize the switching losses. The multi-carrier SPWM control methods also have been implemented to increase the performance of multilevel inverters and have been classified according to vertical or horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as Phase Dissipation (PD), Phase Opposition Dissipation (POD), and Alternative Phase Opposition Dissipation (APOD), while horizontal arrangement is known as phase shifted (PS) control technique. In fact PS-PWM is only useful for cascaded H-bridges and flying capacitors, while PD-PWM is more useful for NPC. Each of the mentioned multi-carrier SPWM control techniques have been illustrated in Fig.6, respectively. The sinusoidal SPWM is the most widely used PWM control method due to many advantages including easy implementation, lower harmonic outputs according to other techniques, and low switching losses. In SPWM control, a high frequency triangular carrier signal is compared with a low frequency sinusoidal modulating signal in an analog or logic. Comparator devices. The frequency of modulating sinusoidal signal defines the desired line voltage frequency at the inverter output.

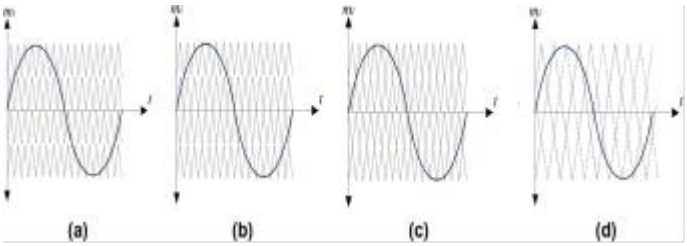

Fig. 6. Multi-carrier SPWM control strategies: (a) PD, (b) POD, (c) APOD, (d) P

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3.2 Space vector Pulse Width Modulation (SVM)

An alternative popular control method for multilevel inverters is defined as space vector PWM (SVM) that directly uses the control variable given by the control system and identifies each switching vector as a point in complex space of (α, β).The harmonic elimination and fundamental voltage ratios in SVM schemes are obtained in better values compared to SPWM schemes. In addition to this, the maximum peak value of the output voltage is 15% greater than triangular carrier-based modulation techniques. Sector identification and look-up table requirement to determine the switching intervals for all vectors make SVM method quite complicated. Although the difficulty of determining sectors and switching sequences according to increased n-level of inverter, DSP and microprocessor implementations provide proper solution while preparing the algorithms The SVM method uses a number of level-shifted carrier waves to compare with the reference phase voltage signals when applied to multilevel inverters. Any three-phase n-level space vector diagram consists of six sectors that all contains (n-1)2 vector combinations per sector and n3 switching. Fig. 7 shows the space vector diagram of a three-phase three-level inverter. Each phase leg of inverter includes four switching devices and has three different switching states that are represented as 1, 0, or -1 to illustrate positive, zero, and negative switching sequences. The switching states have been shown on vector intersections and 27 different states have been located to illustrate required switching states. The switching states and definitions for output voltage levels are given in Table 1. The zero voltage vectors has three switching states as (0 0 0, 1 1 1, -1 -1 -1). The vectors given in Fig. 7 are classified into three groups that are named as small vectors (V1 -V6), middle vectors (V8, V10, V12, V14, V16, V18), and the large vectors (V7, V9, V11, V13, V15, V17). By assuming the reference voltage vector Vref located in the 2nd region (Δ2) of S1 sector, it can be constituted by voltage vectors of V1, V2, and V8 during the sampling period (Ts). The reference voltage also depends on the dwelling times of voltage vector. Hence, the equation for ON time of the voltage vectors that constitutes the reference voltage can be given as in Eq.(1)

$$Vref..Ts=V1.ta+V2.tb+V8.tc \quad (1)$$

ON times of voltage vectors can be determined using Eq. (1) as given in Eq. (2);

$$\left.\begin{aligned} ta&=Ts-2n\sin\theta \\ tb&=2n\sin(\pi/3-\theta)-Ts \\ tc&=Ts-2n\sin(\pi/3+\theta) \end{aligned}\right\} \quad (2)$$

Where $n=(4\sqrt{3}/3)(Vref/Vdc)\,Ts$

The calculations given above has been performed to show one of the possible Vref value in a region of sectors and required to reply to determine each switching sequence. There are various studies have been realized to reduce complicated calculations of vectors, and simplify the required SVM algorithms in order

to control multilevel inverters that generate five-level and above output voltage

Table-2
Switching states and definitions for SVM

Switching symbol	Switching states						Phase voltage
	S_1	S_2	S_1'	S_2'	D_1	D_2	
1	ON	ON	OFF	OFF	OFF	OFF	$V_{dc/2}$
0	OFF	ON	ON	OFF	Depends on load voltage		0
-1	ON	OFF	ON	ON	OFF	OFF	$V_{dc/2}$

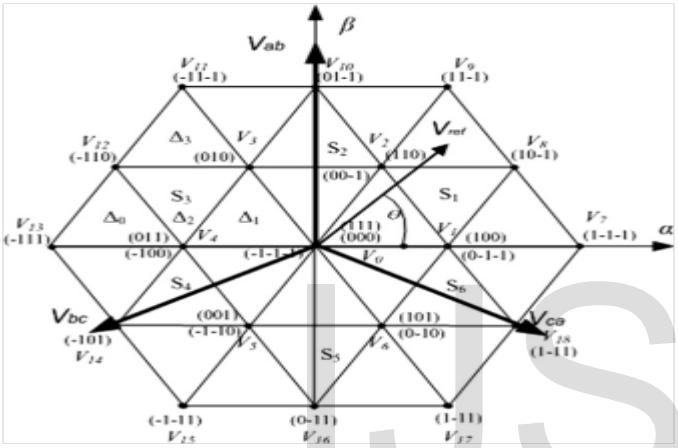


Fig.7. Space vector diagram of a three-level inverter with sector and subsectors

4 SIMULATION RESULT

Simulation of 3-phase, 3-level H Bridge inverter using SVPWM technique is performed in MATLAB/SIMULINK the results are discussed. Simulation is carried out for 3 different modulation index(MI=0.42, 0.5306,0.8596) and the results are discussed here

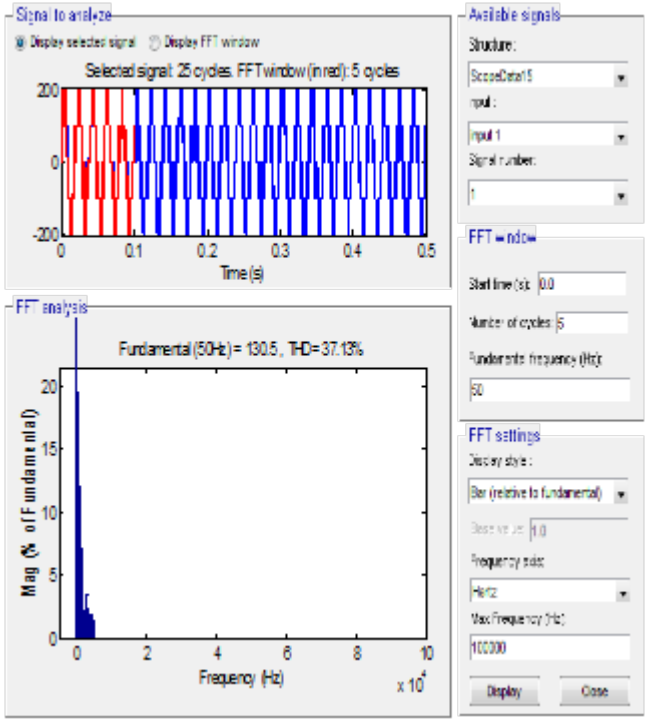


Fig 8.FFT analysis for modulation index=0.42

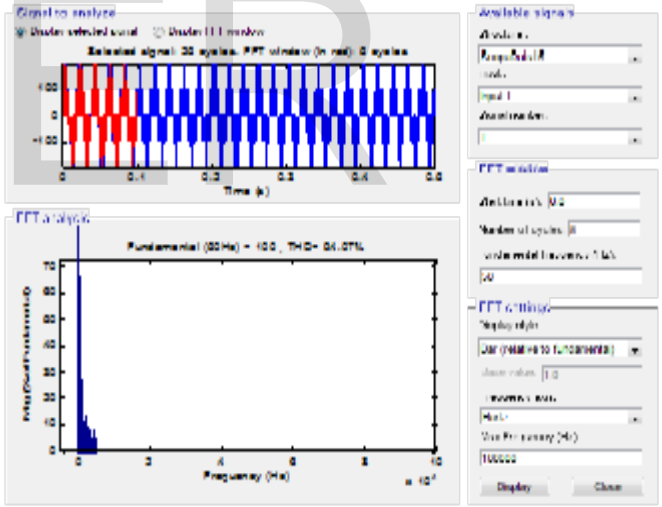


Fig 9.FFT analysis for modulation index=0.530

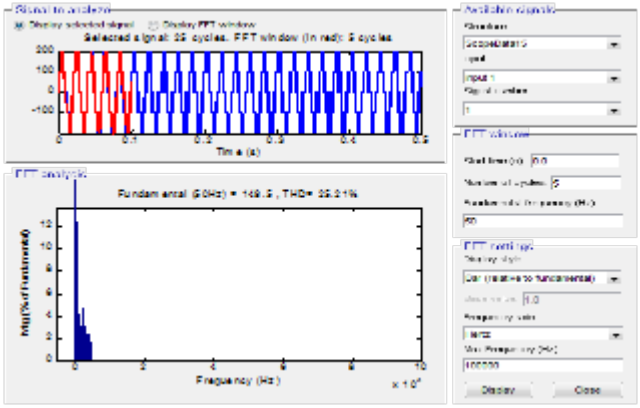


Fig 10.FFT analysis for modulation index=0.8596

TABLE-3

LINE TO LINE VOLTAGES FUNDAMENTAL VALUE RESULTS

Modulation Index	$V_{L\text{-}Fundamental}$ (V)	%THD
0.44	100	94.07
0.5306	130.5	37.13
0.8596	149.5	25.21

In the laboratory a three-level diode clamed inverter prototype is built and THD analysis for different modulation index have been done which is given as follows.

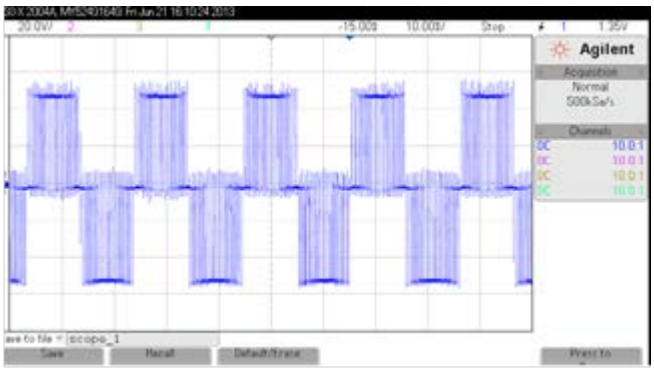


Fig. 11: Phase voltage waveform

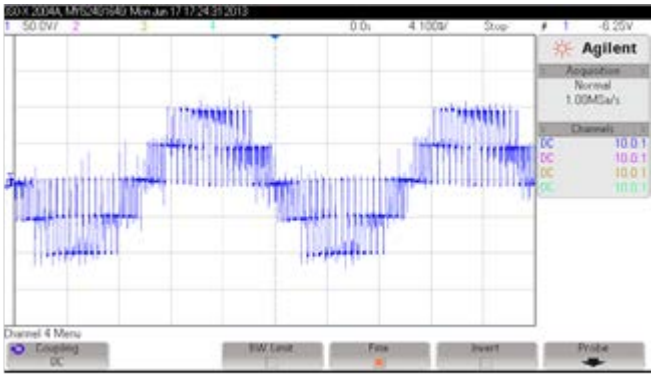
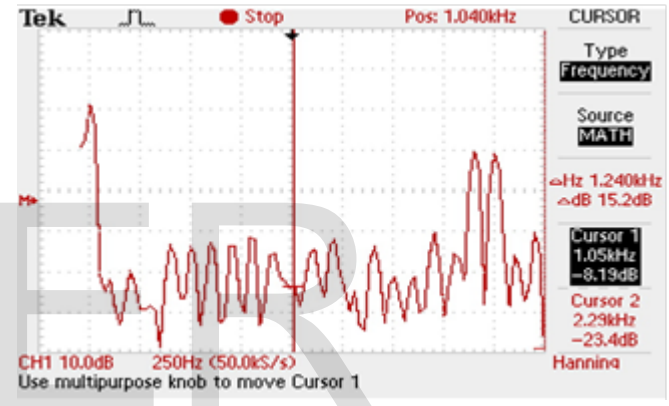


Fig. 12: Line voltage wave form

Figure 13 to 16 shows the FFT analysis of the inverter output voltage for different modulation indices.



.Fig13. FFT window for line to line voltage and 0.9 modulation index

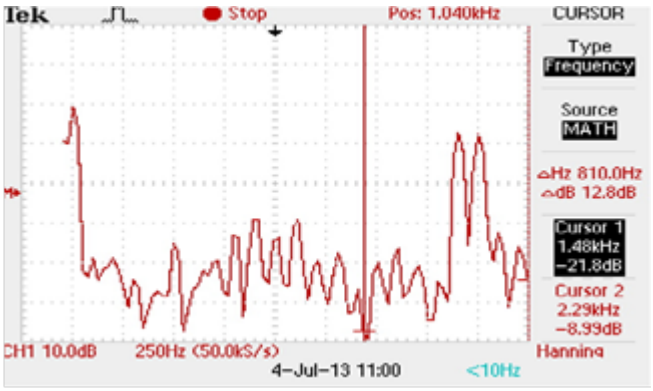


Fig14.FFT window for line to line voltage and 0.8 modulation index

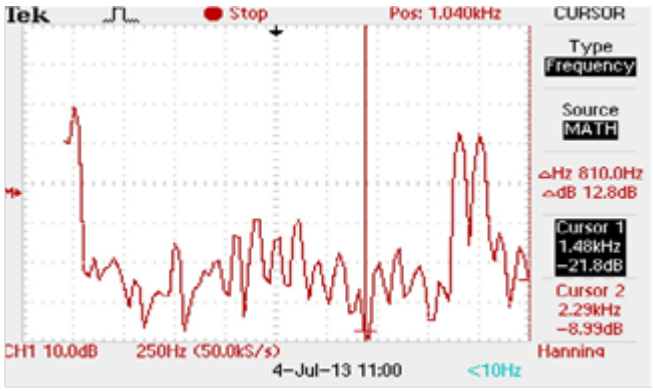


Fig15. FFT window for line to line voltage and 0.7 modulation index

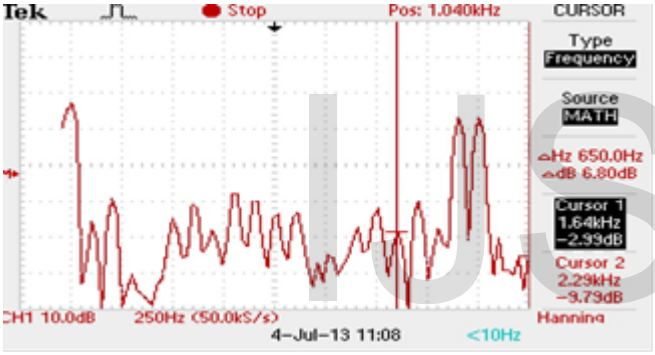


Fig.16. FFT window for line to line voltage and 0.6 modulation index

TABLE-4
LINE TO LINE VOLTAGES FUNDAMENTAL VALUE RESULTS

Modulation Index	Rms Output Voltage	Rms Fundamental Voltage	%THD
0.9	74.8	67.66	47.6
0.8	71.09	58.8	67.9
0.7	66.89	53.7	74.26
0.6	61.6	42.6	104.4

5 RESULTS AND DISCUSSION

In Table 4, there are four different modulation indices arranged in increasing order of magnitude. As in the SPWM technique, a lower modulation index has a higher THD (%).Compared to SPWM with the same modulation index, the THD of SVPWM is slightly lower. The fundamental voltages (Fund) of both techniques are the same. As seen from the simulation results, SVPWM have a superior performance compared to SPWM, especially in the over-modulation region of SVPWM. The SPWM technique is very popular for industrial converters. It is the easiest modulation scheme to understand and implement. This technique can be used in single-phase and three-phase inverters. The SVPWM is significantly better than SPWM by approximately15:5%.Advantages of this method include a higher modulation index, lower switching losses, and less harmonic distortion compared to SPWM However, the SVPWM technique is complex in implementation, especially in the over-modulation region

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